Novel low-voltage, low-power Gb/s transimpedance amplifier architecture

Drew Guckenberger*, Kevin Kornegay
Advanced Integrated Microsystems Research Group, School of Electrical and Computer Engineering, Cornell University, Ithaca, NY, USA, 14853-5401.

ABSTRACT

A novel current-mode transimpedance amplifier (TIA) architecture is proposed for optical receivers. This new architecture, based around the use of a uniquely biased common-base current buffer stage, allows stable, DC coupled TIAs to be designed in bipolar or CMOS processes operating from extremely low supply voltages and using very low levels of power. Noise performance is comparable to that of higher power designs that operate from higher supply rails. Simulation results have been obtained for a 47GHz f_T SiGe BiCMOS process and also 0.25μm CMOS.

Keywords: Transimpedance Amplifier (TIA), Optical Receiver, Low-Voltage, Low-Power, DC Coupled

1. INTRODUCTION

Current trends toward the integration of electro-optic interfaces with high-speed digital ICs, for LANs, SANs and other short-haul applications[1], require low-voltage interface circuits that can operate from the available digital supplies. In order to make arrays of these interconnects efficient and a feasible alternative to electrical interconnects, low power consumption must also be achieved. [2] To meet these requirements, new circuit topologies are required.

Traditional TIA designs typically use a voltage gain stage with resistive negative feedback as a transimpedance amplifier, as shown in Figure 1.[3] This approach has some deficiencies for low-power, low-voltage systems at high data rates.

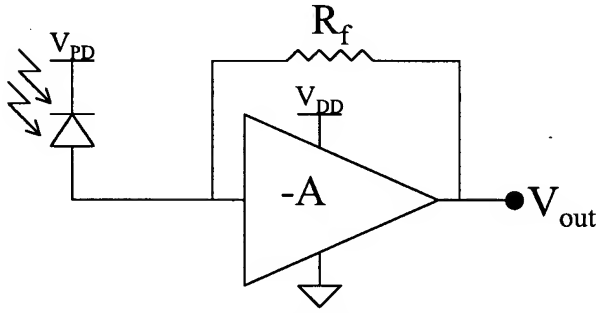


Figure 1: Traditional transimpedance amplifier architecture

The main problem with this approach is that, for correct operation, the input impedance of the voltage gain stage must be large and the transimpedance amplifier input impedance is thus set by the feedback resistance, which is approximately the transimpedance for a sufficiently large voltage gain (A). This means that the circuit's frequency response has a pole at the input node created by the feedback resistance and the photodiode capacitance. Equivalent input noise is another crucial performance metric for any TIA, as it sets the sensitivity limit for the receiver. As R_f decreases, to increase the frequency of the input pole for a fixed photodiode (PD) capacitance, the input noise increases. Therefore, a trade-off must be made in this TIA configuration between sensitivity/gain and bandwidth. Finally, the performance of such systems is limited by the performance of the voltage gain stage, which strongly effects the power consumption, the bandwidth and the required power supply voltage for the overall TIA.

* jag66@cornell.edu; phone 1 607 255-1418; http://aims.ece.cornell.edu/drew

Some CMOS designers have suggested using a common gate (CG) stage as a current buffer at the input[4], as depicted in Figure 2. This configuration presents an input impedance of $1/g_m$ to the photodiode and allows the feedback resistance to be increased, as its effect is now seen by a node with a smaller capacitance.

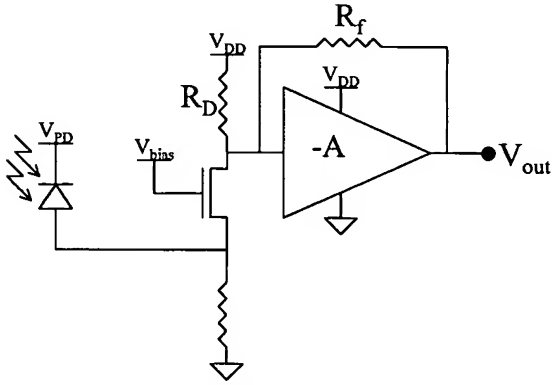


Figure 2: CG input stage based TIA

The concern with this configuration is that a bias current path for the CG stage must still be provided and the bias path input impedance (R_D) must be much greater than the feedback resistance so that the gain is not impaired by the resulting current division. In this way, R_f is still limited by the maximum bias resistor value (R_D) that can be used for the given V_{DD} and current requirements. A solution to this problem is to use the bias resistor directly as the transimpedance resistor. In this way the maximum gain can be achieved and the overall power consumption can be dramatically reduced, by eliminating the voltage gain stage.

A further complication with this topology is finding a way to provide a proper bias for the CG stage over the wide range of input current levels that will be seen if the PD is DC coupled to the TIA. This problem is amplified by the exponential response of the current to V_{be} variations in a bipolar technology, which may make it difficult to sustain a constant collector current in a common base (CB) stage configuration with variations in DC photodiode current for a DC coupled system. The proposed TIA architecture is designed to address this problem.

2. PROPOSED ARCHITECTURE

The proposed bipolar and CMOS architectures are shown in Figure 3 a) and b), respectively. In the subsequent discussion only the bipolar case in Figure 3 a) will be discussed for clarity, but the conclusions apply equally well to the CMOS case shown in Figure 3 b). Any significant differences in the CMOS case are noted in the discussion.

DC coupling is desirable for short-haul systems, as coding results in undesired overhead (latency, power and chip area) and therefore the low frequency (LF) cut-off of the TIA must be as close to DC as possible to avoid baseline wander and ISI that would result from Fourier components of the signal falling below the LF cut-off. DC coupling can present problems due to variations in the DC input current with input signal power level affecting the bias conditions of the TIA. As such, a topology that is insensitive to these variations over a reasonable range of input power levels is desired. The solution is to provide a path for the DC current without effecting the TIA operating point. This is achieved in the proposed topology, where DC photodiode current variations are shunted through R_B. This increases the DC level of the input node, but by floating the current reference relative to this node, the current through the CB stage is held constant maintaining the DC bias level and the common-mode voltage at the output. Only slight variations are seen due to channel-length modulation effects in the MOSFETs as V_{DS} varies.

In this architecture, the photodiode capacitance sees an input impedance of $1/g_{m0}$, just as with the configuration shown in Figure 2, as Q0 is a common base stage (due to the large capacitor at the base node). Further, the current through Q0, which sets the g_m for the device, is held constant by the current mirror with Q1. By tying the emitters of Q1 and Q0 together, and in turn tying them to the photodiode anode, the collector current in Q0 is held constant regardless of

variations in the photodiode DC current level, which will change the current through R_B and shift the input node DC voltage, without affecting the collector current. In this way Q0's input impedance is held constant, as R_{in} is set by the current and physical characteristics of the transistors. The output DC voltage is also kept constant despite variations in the photodiode DC current, as the DC current through R_T is held constant and hence so is the DC voltage drop across it. As such, the TIA's overall performance is relatively insensitive to variations in the DC current from the PD, as long as:

$$V_{DD} > (I + I_{DC})R_B + \max(V_{be} + V_{ds(sat)}, V_{ce(sat)} + IR_T), \quad (1)$$

in the bipolar case and:

$$V_{DD} > (I + I_{DC})R_B + \max(V_T + V_{ds(sat)}, V_{ds(sat)} + IR_T), \quad (2)$$

in the CMOS case.

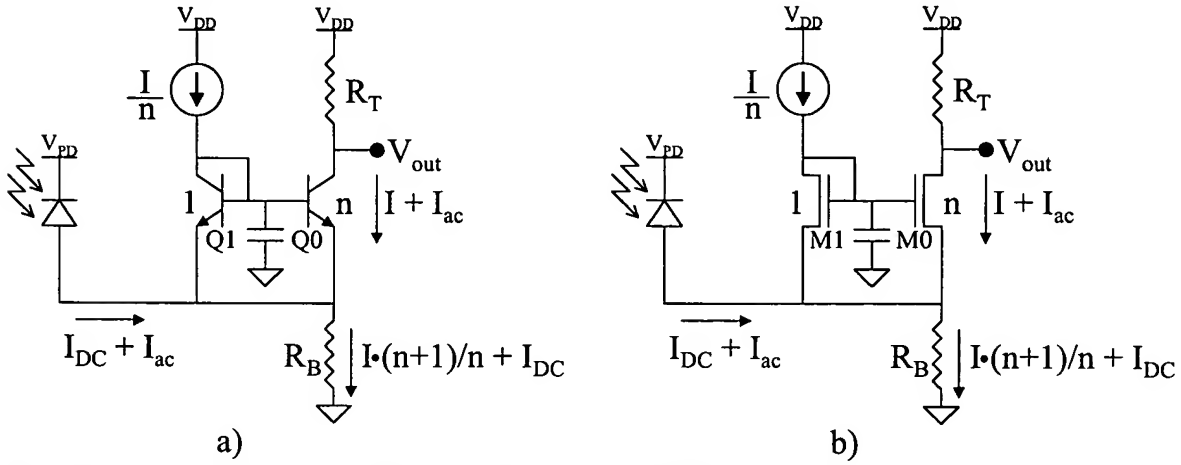


Figure 3: Proposed TIA architecture a) bipolar implementation, b) CMOS implementation

By setting a ratio of n between the sizes of current mirror transistors, the excess bias current from Q1 can be minimized and the input impedance of Q1 can be set large enough to avoid degrading the Q0 signal current transfer (Q1's input impedance will be approximately n times Q0's due to their collector current ratio). For sufficiently large $R_E \| r_{e1}$, most of the signal current will travel through Q0 to the load.

R_B should be set as large as possible, to avoid excess noise, while still providing sufficient DC reverse bias for the photodiode and keeping Q1 in the forward active region over all photodiode DC operating currents. It should be noted that gain is not a function of collector current in this configuration. To get a reasonable input impedance for the TIA (setting an appropriate input pole) requires less than 1mA of collector current in a bipolar implementation for 10Gb/s operation and similar current levels can be used in a CMOS implementation. At I_c=1mA, r_{e0}=25.8Ω at room temperature for a BJT. As such, the entire TIA can be operated using only ~1mA of current, which is much less than typical TIAs. This decreases power consumption and also the voltage drop across the resistors in the circuit, allowing them to be made larger to decrease noise or allowing the supply voltage to be scaled.

Terminating directly into R_T, rather than the feedback resistor and the bias load, as is done in Figure 2, also allows a larger Z_T to be achieved for a given V_{DD} than with the approach followed in Figure 2.

It should be noted that resistors are used for R_B and R_T instead of MOSFETs to bias the circuit or provide active loads. This is due to the their noise advantage. If we compare the noise of a resistor to that of a MOSFET, it can be found that the resistor provides lower noise (for a given Vds or voltage drop across the resistor) unless:

$$Vgs - Vt > 2\Gamma Vds, \tag{3}$$

where Γ is the excess noise factor (2/3 in long-channel devices and larger in short channel devices). But for a MOSFET in saturation we require:

$$Vgs - Vt < Vds. \tag{4}$$

Thus, a MOSFET in saturation always generates more noise as a load than an equivalent resistor. Therefore, resistors are used for R_B and R_T. This is feasible because the bias has been set at the base of the CB amplifier stage.

The main advantages of this architecture are that it can be DC coupled (with stable performance over a wide range of DC input currents), its low power requirements and the feasibility of scaling the power supply voltage due to the low current draw.

3. THEORETICAL ANALYSIS

The complete TIA circuit, including a simple bias generation scheme and photodiode equivalent model can be seen in Figure 4 for the bipolar case. An equivalent circuit is used for the CMOS case. L_{BW} represents bondwire inductance and C_{BP} is bondpad capacitance.

Due to the characteristic temperature stability of this TIA architecture, which will be illustrated later, only a simple resistive bias generation scheme has been required for stable performance over temperature.

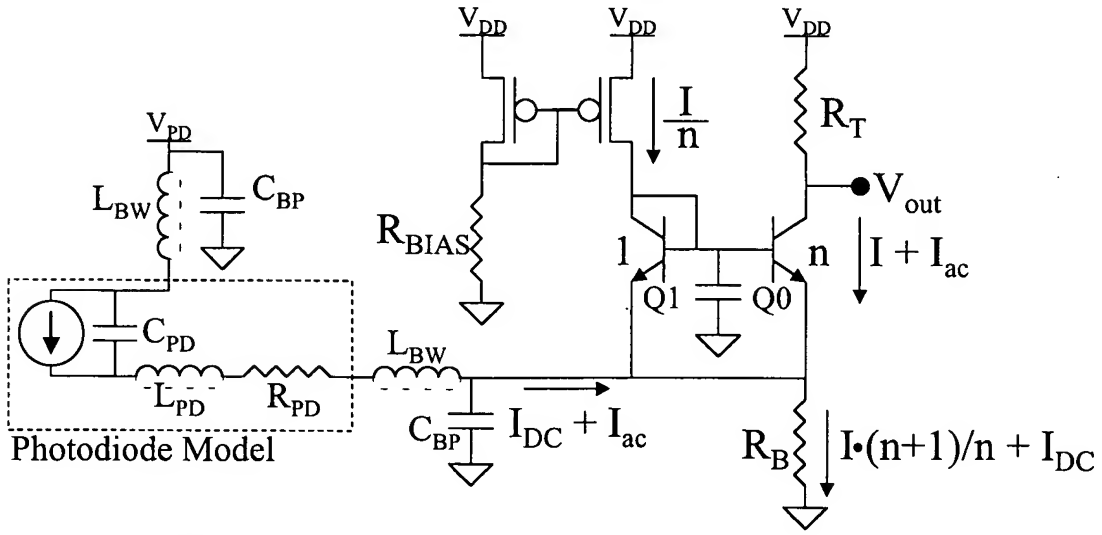
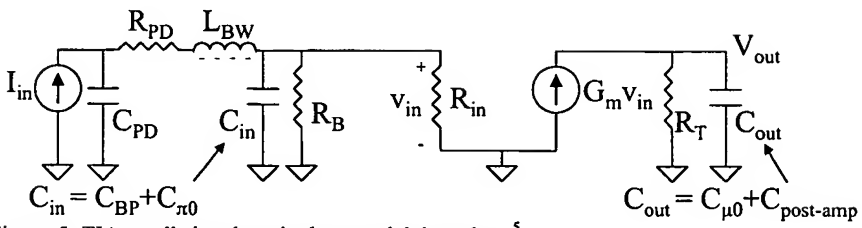


Figure 4: Complete bipolar TIA circuit with PD model included

3.1. Frequency response

The TIA small signal equivalent model is shown in Figure 5.



	MOSFET	BJT
R_{in}	$\frac{1}{g_m + g_{mb}}$	$\frac{\alpha_o}{g_m}\left[1+\frac{r_b}{r_\pi}\right] \approx \frac{1}{g_m}$
G_m	$g_m + g_{mb}$	$\frac{g_m}{\left[1+\frac{r_b}{r_\pi}\right]} \approx g_m$
α_o	1	$\frac{\beta_o}{\beta_o+1} \approx 1$

Figure 5: TIA small signal equivalent model, based on [5]

Using this model, the broadband transimpedance gain of the circuit can be found to be:

$$Z_{T_o} = \frac{V_{out}}{I_{in}} = R_T G_m \frac{R_B R_{in}}{R_B + R_{in}}. \tag{5}$$

Which, in the CMOS case simplifies to:

$$\left(Z_{T_o}\right)_{CMOS} = R_T \left[\frac{R_B}{R_B + \frac{1}{g_m + g_{mb}}}\right] \approx R_T \text{ for } R_B >> \frac{1}{g_m + g_{mb}}, \tag{6}$$

and in the bipolar case simplifies to:

$$\left(Z_{T_o}\right)_{Bipolar} = R_T \alpha_o \left[\frac{R_B}{R_B + \frac{\alpha_o}{g_m}\left[1+\frac{r_b}{r_\pi}\right]}\right] \approx R_T \text{ for } \beta_o >> 1,\ R_B >> \left(\frac{\alpha_o}{g_m}\left[1+\frac{r_b}{r_\pi}\right] \approx \frac{1}{g_m}\right). \tag{7}$$

It should be noted that in both cases,

$$\frac{\partial Z_{T_o}}{\partial T} \cong \frac{\partial R_T}{\partial T}. \tag{8}$$

Therefore, only the temperature coefficient of R_T affects the broadband gain significantly. By using a polysilicon resistor with a low temperature coefficient of resistivity (TCR), a very stable thermal response can be achieved.

From the model in Figure 5, the transimpedance frequency response can be calculated as:

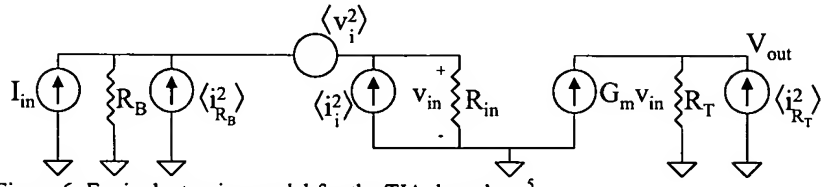
$$Z_T \cong Z_{T_o}\left[\frac{1}{1+sR_TC_{out}}\right]\left[\frac{1}{1+(R_{PD}+R_{in})C_{PD}s+L_{BW}C_{PD}s^2}\right], \text{ for } \left|\frac{1}{j\omega C_{in}}\right| >> R_{in}, \tag{9}$$

over the frequency range of interest.

This is a three pole system. The collector current of Q0 is selected such that the dominant pole is at the output (R_CC_{out}). However, the input complex poles have an important effect on the transient response overshoot and settling time.

3.2. Noise analysis

A simplified noise model for the TIA is shown in Figure 6. This model neglects the noise effects of Q1, since they are assumed small. This assumption has been confirmed through more rigorous calculations and simulation.



	MOSFET	BJT
$\frac{<v_i^2>}{\Delta f}$	$\frac{4kT\cdot\Gamma}{g_m}$	$4kT\left(r_b+\frac{1}{2g_m}\right)$
$\frac{<i_i^2>}{\Delta f}$	$2qI_G+\frac{4kT(\omega C_G)^2\cdot\Gamma}{g_m}$	$2q\left(I_B+\frac{I_C}{\lvert\beta(j\omega)\rvert^2}\right)$

Figure 6: Equivalent noise model for the TIA, based on [5]

Based on this model the equivalent input noise can be calculated as:

$$< i_{in}^2 >= \left[\frac{R_B+R_{in}}{\alpha_o R_B}\right]^2 < i_{R_T}^2 > + < i_{R_B}^2 > + < i_i^2 > + \frac{< v_i^2 >}{R_B^2}. \tag{10}$$

In the CMOS case, neglecting $\frac{1}{f}$ noise, this becomes:

$$\frac{< i_{in}^2 >}{\Delta f} = 4kT\left[\frac{1}{R_T}\left(\frac{R_B+R_{in}}{R_B}\right)^2+\frac{1}{R_B}+\frac{qI_G}{2kT}+\frac{\omega^2C_{GS}^2\Gamma}{g_m}+\frac{1}{R_B^2}\frac{\Gamma}{g_m}\right], \tag{11}$$

and in the bipolar case, again neglecting $\frac{1}{f}$ noise, the noise is expressed as:

$$\frac{< i_{in}^2 >}{\Delta f} = 4kT\left[\frac{1}{R_T}\left(\frac{R_B+R_{in}}{\alpha_o R_B}\right)^2+\frac{1}{R_B}+\frac{q}{2kT}\left(I_B+\frac{I_C}{|\beta(j\omega)|^2}\right)+\frac{1}{R_B^2}\left(r_b+\frac{1}{2g_m}\right)\right]. \tag{12}$$

The integrated noise in the CMOS case can thus be expressed as:

$$\left(I_{noise}^2\right)_{CMOS} = \int_0^{2\pi B} \frac{< i_{in}^2 >}{\Delta f}\frac{d\omega}{2\pi} = 4kTB\left[\frac{\left(R_B + R_{in}\right)^2}{R_T R_B^2} + \frac{1}{R_B} + \frac{qI_G}{kT} + \frac{1}{R_B^2}\frac{\Gamma}{G_m} + \frac{C_{GS}^2\left(2\pi B\right)^2\Gamma}{3G_m}\right], \tag{13}$$

where B is the circuit bandwidth.

The integrated noise in the bipolar case can be expressed as:

$$\left(I_{noise}^2\right)_{Bipolar} = \int_0^{2\pi B} \frac{< i_{in}^2 >}{\Delta f}\frac{d\omega}{2\pi} = 4kTB\left[\frac{\left(R_B + R_{in}\right)^2}{\alpha_o^2 R_T R_B^2} + \frac{1}{R_B} + \frac{qI_B}{2kT} + \frac{1}{R_B^2}\left(r_b + \frac{1}{2g_m}\right)\right]$$
$$+ 2qI_C B\left[\frac{1}{\beta_o^2} + \frac{\left(2\pi B\right)^2}{3\omega_T^2}\right]. \tag{14}$$

Based on equations (13) and (14), we wish to find the optimum transistor size to minimize noise. Therefore, we set $N = \frac{W}{W_o}$, where W_o is an arbitrary normalization width for which G_{mo}, C_{GSo}, $C_{\mu o}$ and r_{bo} are defined, such that:

$$\left(G_m\right)_{CMOS} = G_{mo}\cdot\sqrt{\frac{W}{W_o}} = G_{mo}\cdot\sqrt{N}, \quad C_{GS} = C_{GSo}\cdot\frac{W}{W_o} = C_{GSo}\cdot N, \quad r_b = r_{bo}\cdot\frac{W_o}{W} = \frac{r_{bo}}{N},$$
$$C_\mu = C_{\mu o}\cdot\frac{W}{W_o} = C_{\mu o}\cdot N, \text{ and } R_T = \frac{1}{\omega_{out}\left(C_\mu + C_{post-amp}\right)} = \frac{1}{\omega_{out}\left(NC_{\mu o} + C_{post-amp}\right)}. \tag{15}$$

where ω_{out} is the angular frequency of the (dominant) output pole.

Assuming device length is un-scaled in all cases and neglecting the scaling of leakage current I_G with transistor size in the CMOS case, we can find optimum transistor sizes for each case by substituting (15) into (13) and (14) and solving:

$$\frac{\partial}{\partial N}\left(I_{noise}^2\right) = 0. \tag{16}$$

Which results in:

$$\left(N_{opt}\right)_{CMOS} \cong \frac{1}{2\pi B R_B C_{GSo}} \text{ for } R_T >> R_B, \tag{17}$$

$$\left(N_{opt}\right)_{Bipolar} \cong \frac{1}{R_B + \frac{1}{G_m}}\sqrt{\frac{r_{bo}}{C_{\mu o}\omega_{out}}} \cong \frac{1}{R_B}\sqrt{\frac{r_{bo}}{C_{\mu o}\omega_{out}}}. \tag{18}$$

Next we wish to find the optimum current to minimize noise, so we solve:

$$\frac{\partial}{\partial I}\left(I_{noise}^2\right)=0. \tag{19}$$

In the CMOS case we find that there is no optimum noise current. That is, the higher the current is, the lower the noise is, which makes sense for a current based signal. In the bipolar case, where shot noise in the base is significant, we find that the current that yields the minimum noise is given by:

$$\left(I_{opt}\right)_{Bipolar} \cong \frac{kT\sqrt{\beta}}{qR_B}. \tag{20}$$

This value may not be simultaneously achievable with the G_m required to set the input pole at the desired level, as G_m is a function of current. However, the result will give an indication of how close to optimum noise performance the required current value is.

4. SIMULATION RESULTS

Two TIAs have been designed, based on the analysis above, to the demonstrate performance achievable with this architecture. One TIA is designed in 0.25μm CMOS and one in a SiGe BiCMOS technology with 47GHz f_T HBTs. Both TIAs operate beyond 10Gb/s in a non-return to zero (NRZ) coded system. A photodiode capacitance of 280fF and a bondwire inductance of 750pH have been used for all simulations. Transient simulations use an extinction ratio of 5 (the ratio of the '1' current to the '0' current) and sensitivities are calculated using that extinction ratio and a photodiode responsivity of 0.9A/W for a BER of 10^{-9}.

4.1. 0.25μm CMOS implementation

Simulation results for the TIA implemented in 0.25μm CMOS show 10Gb/s operation with an input referred noise density of 14.6 $pA/\sqrt{Hz}$, drawing less than 1mA from a 1.5V supply. The simulated gain is 42.9dBΩ with a -3dB frequency of 8.5GHz. This represents the highest data rate reported for a TIA in 0.25μm CMOS.

Performance plots are shown in Figure 7 and performance metrics are summarized in Table 3. The eye diagrams demonstrate the insensitivity of the transient response to variations in the input power level. Temperature and supply corner simulations were performed and the results are summarized in Table 2. These results show very good thermal stability, as expected from the analysis.